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EXAMINER	
AHMED, SALMAN	

ART UNIT	PAPER NUMBER
2419	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,848	FAIRMAN, BRUCE ALAN	
	Examiner	Art Unit	
	SALMAN AHMED	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/4/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12,14-20,22-26,28-36,38-51,53-61,63-66,68 and 69* is/are rejected.

7)☒ Claim(s) *7,13,21,27,37,52,62 and 67* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-69 are pending.

Claims 7, 13, 21, 27, 37, 52, 62 and 67 are objected.

Claims 1-6, 8-12, 14-20, 22-26, 28-36, 38-51, 53-61, 63-66 and 68-69 are rejected.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8-11, 14-20, 22-25, 28-35, 38-50, 53-61, 63-65, 68 and 69 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa et al. (Design and implementation of DV based video over RTP. Proc. *Packet Video2000*, 2000), hereinafter Ogawa.

Regarding claim 1, Ogawa teaches a Packet processing apparatus, and packet processing method comprising: a. a packetizing one or more data streams into isochronous data packets; b. encapsulating one or more isochronous data packets according to a real- time transport protocol to form a real-time transport protocol data packet; and c. sending the real-time transport protocol data packets from a transmitting device to a receiving device over a non-isochronous compliant network (sections 4-4.1, we implemented IP based DV video transmission system called DV Transport

System(DVTS) using DV/RTP[5][6]. The overview of the DVTS is shown in Fig. 2. The system consists of a Pentium based PC with FreeBSD as an operating system, IEEE1394 device driver and interface[7], and DV/RTP stream sender and receiver application. Both DV/RTP sender and receiver PC have an IEEE1394 interface on the PCI bus. The camcorder connected DV/RTP sender side (Shown in the left side of Fig. 2) creates IEEE1394 encapsulated DV packet stream. The sender application receives the DV stream via PCI IEEE1394 interface card, encapsulates the DV packet of IEEE1394 into RTP, and transmits it to the IP network. The receiver application obtains the IEEE1394 DV packets by reconstructing DV data received using RTP. IEEE1394 header is attached to the reconstructed DV/IEEE1394 packet and transferred to the DV recorder deck via PCI IEEE1394 interface card (Shown in the right side of Fig. 2). The DV recorder deck displays the DV data on the connected display. The DV system we implemented has the advantage that the system can be configured only with highly available standard PCI based PC compatibles, consumer DV camcorder and DV VCR equipment having IEEE1394 interface. In order to use consumer DV devices equipped with IEEE1394 interface, we designed and implemented an IEEE1394 device driver on FreeBSD 3.3[7]. IEEE1394 high speed serial bus system is designed for a packet based shared media computer bus system. The network bandwidth is logically specified from 100Mbps to 3.2Gbps. The goal of IEEE1394 is to integrate and observe various interface and cable specification into only single bus (cable) system, i.e. storage device interface instead of SCSI and IDE, peripheral of parallel and serial, network of ethernet, processor interconnect of VME and also RCA cable of audio and visual equipment.

Heterogeneous speed devices can be connected within a single IEEE1394 physical network, which enables devices are made at the appropriate cost. Three types of transmission mode is provided by IEEE1394; 1)isochronous stream mode for QoS which provides especially strict packet jitter and guaranteed bandwidth without reliable communication, 2) asynchronous stream for best effort without reliability, and 3)asynchronous request for the reliable communication. Data timing in IEEE1394 is shown in Fig 3. Every packet transmission action is brought with 8 kHz time slice whose value corresponds to the fairness unit in the IEEE1394 system. The 8kHz time slice unit is also divided into 6144 time slot for bandwidth management. Isochronous stream transmission would be done by taking the number of time slot the sender requires first, sending a packet whose size is smaller than the time slot at every 8kHz fairness unit. Therefore, the packet jitter of the isochronous stream mode is suppressed in the order of 8kHz (125 micro second), and the condition might be enough for any jitter sensitive high quality packet video system. It is not easy for the legacy packet based shared network system to satisfy such conditions. However, every IEEE1394 LSI chip already supports the isochronous stream mode on its hardware level, and the cost of a chip is less than $20. Consumer DV adopts IEEE1394 as its digital interface standard, although the isochronous stream mode does not ensure reliable communication. When sending DV stream on IEEE1394, the 80 bytes DIF blocks are aggregated to appropriate size, e.g. an IEEE1394 packet of consumer SD DV stream consists of 6 DIF blocks. 8 bytes common isochronous information (CIP) header is prepended to aggregated DV packet).

Regarding claim 2, Ogawa teaches the transmitting device is coupled to a first isochronous compliant network and the receiving device is coupled to a second isochronous compliant network (see figure 2).

Regarding claim 3, Ogawa teaches eaches the first isochronous compliant network and the second isochronous compliant network each comprise an IEEE 1394 compliant bus architecture (see figure 2 IEEE1394 bus).

Regarding claim 4, Ogawa teaches the first isochronous compliant network and the second isochronous compliant network are coupled via the non-isochronous compliant network (see figure 2).

Regarding claim 5, Ogawa teaches teaches the non-isochronous compliant network comprises an Internet Protocol network (see figure 2).

Regarding claim 6, Ogawa teaches teaches the Internet Protocol network comprises an Ethernet/Internet Protocol network (abstract).

Regarding claim 8, Ogawa teaches the real-time transport protocol defines a real-time transport protocol header and a real-time transport protocol data payload for each real-time transport protocol data packet (see figure 1).

Regarding claim 9, Ogawa teaches the real-time transport protocol data payload comprises one or more isochronous cycle records (See Section 4.1).

Regarding claim 10, Ogawa teaches each of the one or more isochronous cycle records comprises zero or more isochronous data packets (See Section 4.1).

Regarding claim 11, Ogawa teaches each isochronous data packet comprises an IEEE 1394 isochronous data packet (See Section 4.1).

Regarding claim 14, Ogawa teaches each real-time transport protocol data packet includes at least a portion of an isochronous cycle record (See Section 4.1).

Regarding claim 15, Ogawa discloses a an apparatus for communicating data strasm, that apparatus comprising: a. means for packetizing one or more data streams into isochronous data packets; b. means for encapsulating one or more isochronous data packets according to a real- time transport protocol to form a real-time transport protocol data packet; and c. means for sending the real-time transport protocol data packets from a transmitting device to a receiving device over a non-isochronous compliant network (sections 4-4.1, we implemented IP based DV video transmission system called DV Transport System(DVTS) using DV/RTP[5][6]. The overview of the DVTS is shown in Fig. 2. The system consists of a Pentium based PC with FreeBSD as an operating system, IEEE1394 device driver and interface[7], and DV/RTP stream sender and receiver application. Both DV/RTP sender and receiver PC have an IEEE1394 interface on the PCI bus. The camcorder connected DV/RTP sender side (Shown in the left side of Fig. 2) creates IEEE1394 encapsulated DV packet stream. The sender application receives the DV stream via PCI IEEE1394 interface card, encapsulates the DV packet of IEEE1394 into RTP, and transmits it to the IP network. The receiver application obtains the IEEE1394 DV packets by reconstructing DV data received using RTP. IEEE1394 header is attached to the reconstructed DV/IEEE1394 packet and transferred to the DV recorder deck via PCI IEEE1394 interface card (Shown in the right side of Fig. 2). The DV recorder deck displays the DV data on the connected display. The DV system we implemented has the advantage that the system

can be configured only with highly available standard PCI based PC compatibles, consumer DV camcorder and DV VCR equipment having IEEE1394 interface. In order to use consumer DV devices equipped with IEEE1394 interface, we designed and implemented an IEEE1394 device driver on FreeBSD 3.3[7]. IEEE1394 high speed serial bus system is designed for a packet based shared media computer bus system. The network bandwidth is logically specified from 100Mbps to 3.2Gbps. The goal of IEEE1394 is to integrate and observe various interface and cable specification into only single bus (cable) system, i.e. storage device interface instead of SCSI and IDE, peripheral of parallel and serial, network of ethernet, processor interconnect of VME and also RCA cable of audio and visual equipment. Heterogeneous speed devices can be connected within a single IEEE1394 physical network, which enables devices are made at the appropriate cost. Three types of transmission mode is provided by IEEE1394; 1)isochronous stream mode for QoS which provides especially strict packet jitter and guaranteed bandwidth without reliable communication, 2) asynchronous stream for best effort without reliability, and 3)asynchronous request for the reliable communication. Data timing in IEEE1394 is shown in Fig 3. Every packet transmission action is brought with 8 kHz time slice whose value corresponds to the fairness unit in the IEEE1394 system. The 8kHz time slice unit is also divided into 6144 time slot for bandwidth management. Isochronous stream transmission would be done by taking the number of time slot the sender requires first, sending a packet whose size is smaller than the time slot at every 8kHz fairness unit. Therefore, the packet jitter of the isochronous stream mode is suppressed in the order of 8kHz (125 micro second), and the condition might

be enough for any jitter sensitive high quality packet video system. It is not easy for the legacy packet based shared network system to satisfy such conditions. However, every IEEE1394 LSI chip already supports the isochronous stream mode on its hardware level, and the cost of a chip is less than $20. Consumer DV adopts IEEE1394 as its digital interface standard, although the isochronous stream mode does not ensure reliable communication. When sending DV stream on IEEE1394, the 80 bytes DIF blocks are aggregated to appropriate size, e.g. an IEEE1394 packet of consumer SD DV stream consists of 6 DIF blocks. 8 bytes common isochronous information (CIP) header is prepended to aggregated DV packet).

Regarding claims 16-20, 22-25 and 28, Ogawa teaches discloses all the limitations as discussed in the rejection of claims 1-11 and 13-14 and are therefore apparatus claims 16-25 and 27-28 are rejected using the same rationales.

Regarding claim 29, Kanehara anticipates apparatus to communicate data streams, the apparatus comprising: • a transmitting circuit (figure 2, DV/RTP sender and receiver PC) configured to encapsulate one or more first isochronous data packets according to a real-time transport protocol, thereby forming a first real-time transport protocol data packet, and to transmit the first real-time transport protocol data packets (Section 4, IEEE1394 device driver and interface[7], and DV/RTP stream sender and receiver application. Both DV/RTP sender and receiver PC have an IEEE1394 interface on the PCI bus. The camcorder connected DV/RTP sender side) creates IEEE1394 encapsulated DV packet stream. The sender application receives the DV stream via PCI IEEE1394 interface card, encapsulates the DV packet of IEEE1394 into RTP, and

transmits it to the IP network); a receiving circuit (figure 2, DV/RTP sender and receiver PC) configured to receive a second real-time transport protocol data packet, and to de-encapsulate the received second real-time transport protocol data packets into one or more second isochronous data packets (Section 4, The receiver application obtains the IEEE1394 DV packets by reconstructing DV data received using RTP. IEEE1394 header is attached to the reconstructed DV/IEEE1394 packet and transferred to the DV recorder deck via PCI IEEE1394 interface card).

Regarding claim 43, Kanehara a network of devices to communicate data streams, the network of devices comprising: a. a transmitting device configured to encapsulate one or more isochronous data packets according to a real-time transport protocol, thereby forming a real-time transport protocol data packet, and to transmit the real-time transport protocol data packets; b. a first isochronous compliant network coupled to the transmitting device; c. a receiving device configured to receive the real-time transport protocol data packets; d. a second isochronous compliant network coupled to the receiving device; and e. a network coupled to the first isochronous compliant network and the second isochronous compliant network to transmit the real-time transport protocol data packets from the transmitting device to the receiving device; a non-isochronous compliant network coupled to the receiving device; and Saito the same or similar fields of endeavor teaches the use of public network such as internet, and the ATM network exists between them (sections 4-4.1, we implemented IP based DV video transmission system called DV Transport System(DVTS) using DV/RTP[5][6]. The overview of the DVTS is shown in Fig. 2. The system consists of a Pentium based

PC with FreeBSD as an operating system, IEEE1394 device driver and interface[7], and DV/RTP stream sender and receiver application. Both DV/RTP sender and receiver PC have an IEEE1394 interface on the PCI bus. The camcorder connected DV/RTP sender side (Shown in the left side of Fig. 2) creates IEEE1394 encapsulated DV packet stream. The sender application receives the DV stream via PCI IEEE1394 interface card, encapsulates the DV packet of IEEE1394 into RTP, and transmits it to the IP network. The receiver application obtains the IEEE1394 DV packets by reconstructing DV data received using RTP. IEEE1394 header is attached to the reconstructed DV/IEEE1394 packet and transferred to the DV recorder deck via PCI IEEE1394 interface card (Shown in the right side of Fig. 2). The DV recorder deck displays the DV data on the connected display. The DV system we implemented has the advantage that the system can be configured only with highly available standard PCI based PC compatibles, consumer DV camcorder and DV VCR equipment having IEEE1394 interface. In order to use consumer DV devices equipped with IEEE1394 interface, we designed and implemented an IEEE1394 device driver on FreeBSD 3.3[7]. IEEE1394 high speed serial bus system is designed for a packet based shared media computer bus system. The network bandwidth is logically specified from 100Mbps to 3.2Gbps. The goal of IEEE1394 is to integrate and observe various interface and cable specification into only single bus (cable) system, i.e. storage device interface instead of SCSI and IDE, peripheral of parallel and serial, network of ethernet, processor interconnect of VME and also RCA cable of audio and visual equipment. Heterogeneous speed devices can be connected within a single IEEE1394 physical

network, which enables devices are made at the appropriate cost. Three types of transmission mode is provided by IEEE1394; 1)isochronous stream mode for QoS which provides especially strict packet jitter and guaranteed bandwidth without reliable communication, 2) asynchronous stream for best effort without reliability, and 3)asynchronous request for the reliable communication. Data timing in IEEE1394 is shown in Fig 3. Every packet transmission action is brought with 8 kHz time slice whose value corresponds to the fairness unit in the IEEE1394 system. The 8kHz time slice unit is also divided into 6144 time slot for bandwidth management. Isochronous stream transmission would be done by taking the number of time slot the sender requires first, sending a packet whose size is smaller than the time slot at every 8kHz fairness unit. Therefore, the packet jitter of the isochronous stream mode is suppressed in the order of 8kHz (125 micro second), and the condition might be enough for any jitter sensitive high quality packet video system. It is not easy for the legacy packet based shared network system to satisfy such conditions. However, every IEEE1394 LSI chip already supports the isochronous stream mode on its hardware level, and the cost of a chip is less than $20. Consumer DV adopts IEEE1394 as its digital interface standard, although the isochronous stream mode does not ensure reliable communication. When sending DV stream on IEEE1394, the 80 bytes DIF blocks are aggregated to appropriate size, e.g. an IEEE1394 packet of consumer SD DV stream consists of 6 DIF blocks. 8 bytes common isochronous information (CIP) header is prepended to aggregated DV packet).

Regarding claim 58, Ogawa teaches a method of communicating data streams, the method comprising: a. packetizing one or more data streams into IEEE 1394 compliant isochronous data packets; b. encapsulating one or more IEEE 1394 compliant isochronous data packets according to a real-time transport protocol to form a real-time transport protocol data packet; and c. sending the real-time transport protocol data packets from a transmitting device to a receiving device over a non-isochronous compliant network (sections 4-4.1, we implemented IP based DV video transmission system called DV Transport System(DVTS) using DV/RTP[5][6]. The overview of the DVTS is shown in Fig. 2. The system consists of a Pentium based PC with FreeBSD as an operating system, IEEE1394 device driver and interface[7], and DV/RTP stream sender and receiver application. Both DV/RTP sender and receiver PC have an IEEE1394 interface on the PCI bus. The camcorder connected DV/RTP sender side (Shown in the left side of Fig. 2) creates IEEE1394 encapsulated DV packet stream. The sender application receives the DV stream via PCI IEEE1394 interface card, encapsulates the DV packet of IEEE1394 into RTP, and transmits it to the IP network. The receiver application obtains the IEEE1394 DV packets by reconstructing DV data received using RTP. IEEE1394 header is attached to the reconstructed DV/IEEE1394 packet and transferred to the DV recorder deck via PCI IEEE1394 interface card (Shown in the right side of Fig. 2). The DV recorder deck displays the DV data on the connected display. The DV system we implemented has the advantage that the system can be configured only with highly available standard PCI based PC compatibles, consumer DV camcorder and DV VCR equipment having IEEE1394 interface. In order

to use consumer DV devices equipped with IEEE1394 interface, we designed and implemented an IEEE1394 device driver on FreeBSD 3.3[7]. IEEE1394 high speed serial bus system is designed for a packet based shared media computer bus system. The network bandwidth is logically specified from 100Mbps to 3.2Gbps. The goal of IEEE1394 is to integrate and observe various interface and cable specification into only single bus (cable) system, i.e. storage device interface instead of SCSI and IDE, peripheral of parallel and serial, network of ethernet, processor interconnect of VME and also RCA cable of audio and visual equipment. Heterogeneous speed devices can be connected within a single IEEE1394 physical network, which enables devices are made at the appropriate cost. Three types of transmission mode is provided by IEEE1394; 1)isochronous stream mode for QoS which provides especially strict packet jitter and guaranteed bandwidth without reliable communication, 2) asynchronous stream for best effort without reliability, and 3)asynchronous request for the reliable communication. Data timing in IEEE1394 is shown in Fig 3. Every packet transmission action is brought with 8 kHz time slice whose value corresponds to the fairness unit in the IEEE1394 system. The 8kHz time slice unit is also divided into 6144 time slot for bandwidth management. Isochronous stream transmission would be done by taking the number of time slot the sender requires first, sending a packet whose size is smaller than the time slot at every 8kHz fairness unit. Therefore, the packet jitter of the isochronous stream mode is suppressed in the order of 8kHz (125 micro second), and the condition might be enough for any jitter sensitive high quality packet video system. It is not easy for the legacy packet based shared network system to satisfy such conditions. However, every

IEEE1394 LSI chip already supports the isochronous stream mode on its hardware level, and the cost of a chip is less than $20. Consumer DV adopts IEEE1394 as its digital interface standard, although the isochronous stream mode does not ensure reliable communication. When sending DV stream on IEEE1394, the 80 bytes DIF blocks are aggregated to appropriate size, e.g. an IEEE1394 packet of consumer SD DV stream consists of 6 DIF blocks. 8 bytes common isochronous information (CIP) header is prepended to aggregated DV packet).

In regards to claim 30, Ogawa teaches the transmitting device is coupled to a first isochronous compliant network and the receiving device is coupled to a second isochronous compliant network (see figure 2).

Regarding claims 31, 44 and 59 Ogawa teaches the first isochronous compliant network and the second isochronous compliant network each comprise an IEEE 1394 compliant bus architecture (see figure 2 IEEE1394 bus).

Regarding claim 32, Ogawa teaches the first isochronous compliant network and the second isochronous compliant network are coupled via the non-isochronous compliant network (see figure 2).

Regarding claims 33, 56, 64 and 69 Ogawa teaches the real-time transport protocol data payload comprises one or more isochronous (I394) cycle records (See Section 4.1).

Regarding claims 34, 57 and 65 Ogawa teaches each of the one or more isochronous cycle records comprises zero or more isochronous data packets (See Section 4.1).

Regarding claim 35 and 50, Ogawa teaches each isochronous data packet comprises an IEEE 1394 isochronous data packet (See Section 4.1).

Regarding claims 38 and 53, Ogawa teaches the transmitting circuit is further configured to packetize one or more data streams into the one or more isochronous data packets (See section 4).

Regarding claims 39 and 54, Ogawa teaches the transmitting circuit is further configured to receive the one or more isochronous data packets from another device (See sections 4 and 4.1).

Regarding claims 40, 55 and 68, Ogawa teaches the receiving circuit is further configured to parse the one or more isochronous data packets (I394) from each received real-time transport protocol data packet (See sections 4 and 4.1).

Regarding claims 41 and 48 Ogawa teaches each real-time transport protocol data packet includes at least a portion of an isochronous cycle record (See Section 4.1).

Regarding claims 42 and 49, Ogawa teaches each of the one or more isochronous cycle records comprises zero or more isochronous data packets (See Section 4.1).

Regarding claims 45 and 60, Ogawa teaches the non-isochronous compliant network comprises an Internet Protocol network (see figure 2).

Regarding claims 46 and 61 Ogawa teaches the Internet Protocol network comprises an Ethernet/Internet Protocol network (see Abstract).

Regarding claims 47 and 63, Ogawa teaches the real-time transport protocol defines a real-time transport protocol header and a real-time transport protocol data payload for each real-time transport protocol data packet (see figure 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12, 26, 36, 51, and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (Design and implementation of DV based video over RTP. Proc. Packet Video2000, 2000), hereinafter Ogawa as applied to claims 1, 15, 29, 43 and 58 and further in view of Saito et al., hereinafter Saito, (US6523696).

Regarding claims 12 and 26, Ogawa discloses all the subject matter of the claimed invention of claims 1 and 15 with the exception of each IEEE 1394 isochronous data packet includes an IEEE 1394 data payload formatted according to an IEC 61883-1 compliant Common Isochronous Protocol (CIP).

Saito et al. from the same or similar fields of endeavor teaches the use of encapsulation of the IEC 61883 (see Saito et al. column 38 line 2).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the encapsulation of the IEC 61883 as taught by Saito et al in the

packet processing apparatus, and packet processing method of Ogawa in order tot provide necessary rules and guidelines for transmitting data (see Saito column 38 line 5-10 and column 39 line 3-12).

Regarding claims 36, 51, and 66, Ogawa discloses all the subject matter of the claimed invention of claims 29, 43 and 58 with the exception of each IEEE 1394 isochronous data packet includes an IEEE 1394 data payload formatted according to an IEC 61883-1 compliant Common Isochronous Protocol (CIP).

Saito et al. from the same or similar fields of endeavor teaches the use of encapsulation of the IEC 61883 (see Saito et al. column 38 line 2).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the encapsulation of the IEC 61883 as taught by Saito et al in the packet processing apparatus, and packet processing method of Ogawa in order tot provide necessary rules and guidelines for transmitting data (see Saito column 38 line 5-10 and column 39 line 3-12).

Allowable Subject Matter

5. Claims 7, 13, 21, 27, 37, 52, 62 and 67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments see pages 2-8 of the Remarks section, filed 4/4/2008, with respect to the rejections of the claims have been fully considered and are moot in view of the new ground of rejections presented in this office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SALMAN AHMED whose telephone number is (571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Salman Ahmed/

Examiner, Art Unit 2419